IN THE CLAIMS

1. (Currently Amended) A switching fabric for interfacing a host processor and a plurality of network modules, comprising:

a plurality of network module interfaces, each network module interface operable to communicate with one or more associated network modules over a module communication link, the plurality of network modules operable to communicate among one another over a peer transaction bus interconnecting the plurality of network module interfaces;

a processor interface operable to communicate with a host processor over a host communication link, the processor interface operable to communicate with the plurality of network module interfaces over a host transaction bus, the peer transaction bus being separate from the host transaction bus to allow communications between network modules without interfering with host processor communications.

2. (Original) The switching fabric of Claim 1, wherein the module communication link which each of the plurality of network module interfaces communicates with its associated network modules is a Peripheral Component Interconnect (PCI) bus.

3. (Original) The switching fabric of Claim 2, wherein each of the plurality of network module interfaces is operable to convert between a protocol of the PCI bus and protocols of the peer transaction bus and the host transaction bus.

4. (Original) The switching fabric of Claim 1, wherein the host communication link which the processor interface communicates with the host processor is a Peripheral Component Interconnect (PCI) bus.

5. (Original) The switching fabric of Claim 4, wherein the processor interface is operable to convert between a protocol of the PCI bus and a protocol of the host transaction bus.

6. (Original) The switching fabric of Claim 1, further comprising:

a peer transaction bus controller operable to control information transfer across the peer transaction bus;

a host transaction bus controller operable to control information transfer across the host transaction bus.

7. (Previously Presented) A switching fabric for interfacing a host processor and a plurality of network modules, comprising:

a plurality of network module interfaces, each network module interface operable to communicate with one or more associated network modules over a module communication link, the plurality of network modules operable to communicate among one another over a peer transaction bus;

a processor interface operable to communicate with a host processor over a host communication link, the processor interface operable to communicate with the plurality of network module interfaces over a host transaction bus;

wherein each of the plurality of network module interfaces includes:

a network module interface core operable to convert between a protocol of the module communication link between each of the plurality of network module interfaces and their respective network modules and protocols of the peer transaction bus and the host transaction bus;

a peer ingress buffer operable to receive information from an associated network module for transfer onto the peer transaction bus;

a peer egress buffer operable to receive information from a remote network module over the peer transaction bus for transfer to an appropriate associated network module;

a network module write posting buffer operable to receive communications from an associated network module destined for the host processor for transfer onto the host transaction bus;

a network module delayed read buffer operable to receive information from the host processor over the host transaction bus for transfer to an appropriate associated network module.

8. (Previously Presented) A switching fabric for interfacing a host processor and a plurality of network modules, comprising:

a plurality of network module interfaces, each network module interface operable to communicate with one or more associated network modules over a module communication link, the plurality of network modules operable to communicate among one another over a peer transaction bus;

a processor interface operable to communicate with a host processor over a host communication link, the processor interface operable to communicate with the plurality of network module interfaces over a host transaction bus;

wherein the processor interface includes:

a processor interface core operable to convert between a protocol of the host communication link between the host processor and the processor interface and a protocol of the host transaction bus;

a host delayed read buffer operable to receive information from the host processor for transfer to a network module over the host transaction bus;

a processor initiator write buffer operable to receive information over the host transaction bus from a network module for transfer to the host processor.

9. (Previously Presented) A switching fabric for interfacing a host processor and a plurality of network modules, comprising:

a plurality of network module interfaces, each network module interface operable to communicate with one or more associated network modules over a module communication link, the plurality of network modules operable to communicate among one another over a peer transaction bus;

a processor interface operable to communicate with a host processor over a host communication link, the processor interface operable to communicate with the plurality of network module interfaces over a host transaction bus;

wherein a clock driving the host transaction bus and the peer transaction bus is derived from a clock driving the host communication link.

10. (Original) The switching fabric of Claim 1, wherein the host communication link and the module communication links operate at different clock frequencies.

11. (Previously Presented) A switching fabric for interfacing a host processor and a plurality of network modules, comprising:

a plurality of network module interfaces, each network module interface operable to communicate with one or more associated network modules over a module communication link, the plurality of network modules operable to communicate among one another over a peer transaction bus;

a processor interface operable to communicate with a host processor over a host communication link, the processor interface operable to communicate with the plurality of network module interfaces over a host transaction bus;

wherein the peer transaction bus carries layer two traffic and the host transaction bus carries layer three traffic.

12. (Original) The switching fabric of Claim 11, wherein the layer two traffic is in asynchronous transfer mode cells.

13. (Currently Amended) A method for interfacing a host processor and a plurality of network modules, comprising:

providing a module communication link between a network module interface and associated network modules;

providing a peer transaction path between a plurality of the network module interfaces to allow communications between non-associated network modules;

providing a host communication link between a processor interface and a host processor;

providing a host transaction path between the processor interface and the plurality of network ~~interface~~ module interfaces to allow communications between the host processor and all network modules, the peer transaction path being separate from the host transaction path to allow communications between network modules without interfering with the host processor communications.

14. (Original) The method of Claim 13, further comprising:

sending information between the host processor and the processor interface using a Peripheral Component Interface (PCI) bus protocol.

15. (Original) The method of Claim 14, further comprising:

converting the PCI bus protocol to and from a protocol of the host transaction path.

16. (Original) The method of Claim 15, further comprising:

converting the protocol of the host transaction path to and from a protocol of the module communication link.

17. (Original) The method of Claim 16, wherein the protocol of the module communication link is the PCI bus protocol.

18. (Original) The method of Claim 13, further comprising:

sending information between a network module and its associated network module interface using a Peripheral Component Interface (PCI) bus protocol.

19. (Original) The method of Claim 18, further comprising:

converting the PCI bus protocol to and from a protocol of the peer transaction path.

20. (Original) A switching fabric for interfacing a host processor and a plurality of network modules, comprising:

means for providing communications with one or more associated network modules over a module communication link;

means for providing communications among non-associated network modules;

means for providing communications with a host processor over a host communication link;

means for providing communications between the host processor and all network modules.